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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,048	06/24/2003	Jason J. Payne	1826-US	1882

7590 05/26/2006

Teradyne, Inc.
Legal Department
321 Harrison Avenue
Boston, MA 02118

EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,048	PAYNE ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The request filed on 5/18/06 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 10/603048 is acceptable and a RCE has been established. An Action on the RCE follows.

2. The amendment filed on 5/17/06 has been entered. Applicants have amended claim 1 and added new claim 20.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation: **"the routing channel"** announces in claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (US 5331514) in view of McNamara et al. (US 6537087) and further in view of Uematsu et al. (US 6787710).

Regarding claim 1, Kuroda, as can be seen in figures 1, 2, and 5, discloses a PCB having a surface providing a mating interface to which is electrically connected an

electrical component having signal conductors 3S(3) and ground conductors 3G(3), see column 2, lines 28-49. The PCB comprising:

(a) A plurality of stacked dielectric layers 2 with a conductor 3S(3) and 3G(3) exposed on at least one of the plurality of the layers, see column 1, lines 41-43, column 2, lines 21 and 44-49,

(b) a mating interface including:

(c) a plurality of conductive vias 3 (conductive poles) aligned in a repeating pattern of a square so forming a plurality of rows of squares, see figure 5 and column 1, lines 44-53,

(d) the plurality of conductive vias 3 extending through at least a portion of the plurality of the layers 2, at least one of the plurality of conductive vias 3 intersecting the conductor, see column 2, line 62-continuing column 3, line 9,

(e) the plurality of conductive vias 3 including signal conductor connecting conductive vias 3S and ground conductor connecting conductive vias 3G, see column 2, lines 44-49,

(f) wherein, for each of plurality of rows of the conductive vias 3, there are at least twice as many ground conductor connecting conductive vias 3G as signal conductor connecting conductive vias 3S and the conductive vias 3 are positioned relative to one another so that for each signal conductor connecting conductive via 3S, there are ground conductor connecting conductive vias 3G adjacent either side of the signal conductor connecting conductive via 3S, see figure 5 and column 1, lines 49-59.

However, Kuroda does not disclose at least one routing channel positioned between at least two of the plurality of rows.

It is old and known in the art that routing channels are formed in every printed circuit board for electrical connections between terminals providing an open area or region for conductive routing traces to be formed, especially in high-density circuit boards. Generally, the connections are formed in predetermined areas or regions, called channels, within the circuit board.

McNamara et al., as shown in figures 17 and 18 and column 8, lines 18-32, disclose a circuit board 16 having signal contact surface mounting pads 300 and ground contact surface mounting pads 302 inherently formed on respective signal and ground vias (no number, see figure 18). The signal and ground pads are arranged in a plurality of rows 304, 306 and 308; and, for each signal pad, there are ground pads adjacent on either side, thus so the respective vias. McNamara et al. further disclose routing channels 311 formed in between at least two of the plurality of rows for signal routing traces.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from McNamara about the routing channels on the board of Kuroda in order to provide conductive routing traces for electrical connections between the signal conductor connecting conductive vias and responsive signal terminals formed within the board.

Regarding claim 2, Kuroda discloses the vias that can be arranged in a rectangular pattern instead of a square pattern so forming rows of vias along the

corners of the width sides of the rectangular, see column 4, lines 9-17. Since the width of a rectangular is shorter than the length, therefore the distance between the signal conductor connecting conductive via 3S and the adjacent ground conductor connecting conductive via 3G of a row is always less than the distance between adjacent rows of the conductive vias 3.

Regarding claim 3, Kuroda discloses the vias that can be arranged in a square or a rectangular pattern, as explained in claims 1 and 2 above. In a square pattern, the distance between a signal conductor connecting conductive via 3S and an adjacent ground conductor connecting conductive via 3G on one side is similar to a distance between the signal conductor connecting conductive via 3S and an adjacent ground conductor connecting conductive via 3G on the other side.

Regarding claim 4, as can be seen in figure 2, Kuroda discloses a surface mounting pad (no number) disposed on each of the plurality of conductive vias 3, the signal conductor 3S(3) and ground conductor 3G(3) of the electrical component being electrically connected to the surface mounting pads. The surface mounting pads are the top conductive surface of the vias that the component is attached to.

Regarding claim 6, Kuroda discloses every limitation as shown in claim 1 above including a ground and a power plane layer (no number, see column 1, lines 29-48) through which at least some of the plurality of conductive vias inherently extend, but fails to disclose for each signal conductor connecting conductive via of the ground plane layer, there is provided an area surrounding the signal conductor connecting conductive via that is free of the ground plane layer.

Uematsu et al. disclose a PCB having conductive vias 10 and 11 extending through a multilayer substrate, which includes a ground plane layer 2 and an area 14 (insulating portions) surrounding the vias that is free of the layers, see figure 1 and column 3, lines 19-20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the insulating portion as taught by Uematsu et al. in the PCB of Kuroda for preventing short circuit between the signal conductor connecting conductive via and the ground layer.

Regarding claim 7, as can be seen in Kuroda's figure 1 and further in view of Uematsu et al., and as explained in claim 6 above, each ground conductor connecting conductive via of the ground plane layer, there is provided at least one discrete area adjacent the ground conductor connecting conductive via that is free of the ground plane layer, which is the insulating portion provided by signal conductor connecting conductive via.

Regarding claim 8, Kuroda in view of Uematsu et al., discloses every limitation as shown in claims 1, 6, and 7 above, in the same manner as described in claims 6 and 7 where the power plane layer is in place of ground plane layer.

Response to arguments

7. Applicant's arguments with respect to claims 1-4 and 6-9 have been considered but are moot in view of the new ground(s) of rejection. Applicants' arguments:

Remarks, page 12, line 4: The argument is that the Office action has not cited to any specific teachings in support the rejection on claim 2-4.

The argument is not persuasive. Because:

(a) Regarding claim 2, Kuroda discloses in column 4, lines 9-17 that the conductor poles can be arranged in square or other patterns. The Examiner considers the conductor poles formed in rectangular patterns. When conductor poles 3 are formed in row of rectangular patterns, then the distance between the signal conductor connecting conductive via 3S and the adjacent ground conductor connecting conductive via 3G of a row is always less than the distance between adjacent rows of the conductive vias 3. Noted that when the Examiner refers to a specific pattern (square/rectangular), the vias are at the corners of the pattern.

(b) Regarding claim 3, the same reading when applies to a square pattern (all sides are equal creating equal distances between corners).

(c) Regarding claim 4, figure 2 clearly shows pads connecting to the conductor poles (for pads disposed on vias are old and well known)

Remarks, page 13, lines 3-5: The argument is that Kuroda does not disclose or suggest the features of claim 1.

Kuroda does disclose the features of claim 1, because **the claims fail to recite any structure limitation with the regard to the vias that would keep the claims from reading on the interpretation of the reference that a selected group of vias (4 vias) arranged in a square or rectangular pattern formed into rows of squares or row of rectangles.**

Allowable Subject Matter

8. Claim 5 is objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all the limitations of the base claims and any intervening claims.

9. Claims 9-20 are allowed.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
5/25/06

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800